

ABSTRACT

1 Emulation communications via a test access port and
2 boundary-scan architecture providing serial access to a serial
3 connection of a plurality of registers disposed in a plurality
4 of modules. One of the modules is selected for communication.
5 Nonselected modules are made nonresponsive to data on the
6 serial connection. The external emulation hardware supplies a
7 serial signal having a first logic state for a number of
8 cycles greater in number than a number of bits of the serial
9 connection of registers to the test access port. The the
10 emulation hardware supplies a start bit having an opposite
11 logic state. The selected module detects the start bit and
12 stores the next predetermined number of data bits. These bits
13 could be data bits to be stored in a program visible data
14 register or bits interpreted as an instruction for execution
15 by the module. The selected module may transmit return
16 communications via the serial scan path using the same format.

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